

# NP061A3

## Silicon PNP epitaxial planar type

For digital circuits

### ■ Features

- SSS-Mini type 6-pin package, reduction of the mounting area and assembly cost by one half
- Maximum package height (0.4 mm) contributes to develop thinner equipments

### ■ Basic Part Number

- UNR31A3 × 2

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{\text{CBO}}$	-50	V
Collector-emitter voltage (Base open)	$V_{\text{CEO}}$	-50	V
Collector current	$I_{\text{C}}$	-80	mA
Total power dissipation *	$P_{\text{T}}$	125	mW
Junction temperature	$T_{\text{j}}$	125	$^\circ\text{C}$
Storage temperature	$T_{\text{stg}}$	-55 to +125	$^\circ\text{C}$

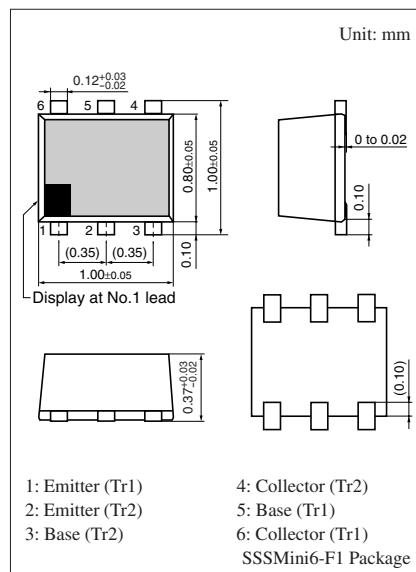
Note) \*: Measuring on substrate at 17 mm × 10 mm × 1 mm

### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{\text{CBO}}$	$I_{\text{C}} = -10 \mu\text{A}$ , $I_{\text{E}} = 0$	-50			V
Collector-emitter voltage (Base open)	$V_{\text{CEO}}$	$I_{\text{C}} = -2 \text{ mA}$ , $I_{\text{B}} = 0$	-50			V
Collector-base cutoff current (Emitter open)	$I_{\text{CBO}}$	$V_{\text{CB}} = -50 \text{ V}$ , $I_{\text{E}} = 0$			-0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{\text{CEO}}$	$V_{\text{CE}} = -50 \text{ V}$ , $I_{\text{B}} = 0$			-0.5	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{\text{EBO}}$	$V_{\text{EB}} = -6 \text{ V}$ , $I_{\text{C}} = 0$			-0.1	mA
Forward current transfer ratio	$h_{\text{FE}}$	$V_{\text{CE}} = -10 \text{ V}$ , $I_{\text{C}} = -5 \text{ mA}$	80			—
$h_{\text{FE}}$ Ratio *	$h_{\text{FE}}(\text{Small} / \text{Large})$	$V_{\text{CE}} = -10 \text{ V}$ , $I_{\text{C}} = -5 \text{ mA}$	0.50	0.99		—
Collector-emitter saturation voltage	$V_{\text{CE(sat)}}$	$I_{\text{C}} = -10 \text{ mA}$ , $I_{\text{B}} = -0.3 \text{ mA}$			-0.25	V
Output voltage high-level	$V_{\text{OH}}$	$V_{\text{CC}} = -5 \text{ V}$ , $V_{\text{B}} = -0.5 \text{ V}$ , $R_{\text{L}} = 1 \text{ k}\Omega$	-4.9			V
Output voltage low-level	$V_{\text{OL}}$	$V_{\text{CC}} = -5 \text{ V}$ , $V_{\text{B}} = -3.5 \text{ V}$ , $R_{\text{L}} = 1 \text{ k}\Omega$			-0.2	V
Input resistance	$R_{\text{I}}$		-30%	47	+30%	$\text{k}\Omega$
Resistance ratio	$R_{\text{I}} / R_{\text{2}}$		0.8	1.0	1.2	—
Transition frequency	$f_{\text{T}}$	$V_{\text{CB}} = -10 \text{ V}$ , $I_{\text{E}} = 1 \text{ mA}$ , $f = 200 \text{ MHz}$		80		MHz

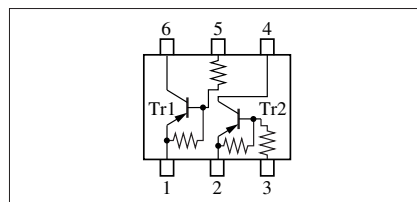
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

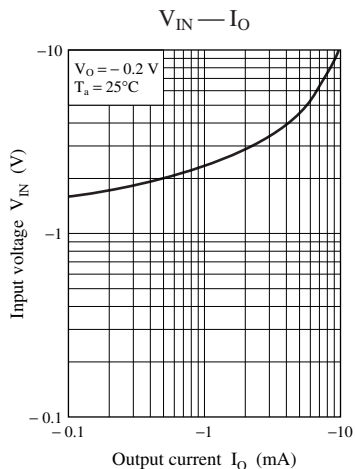
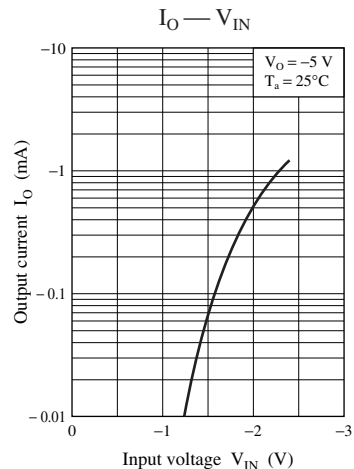
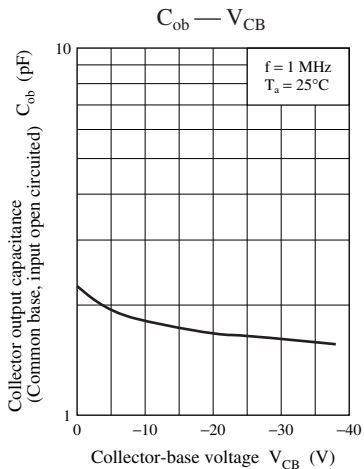
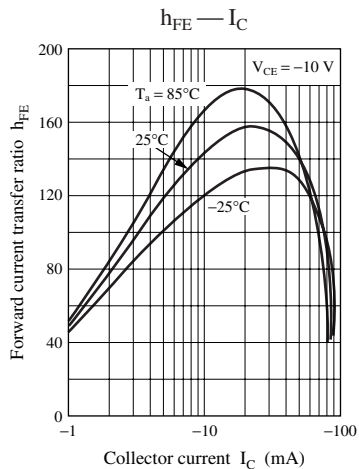
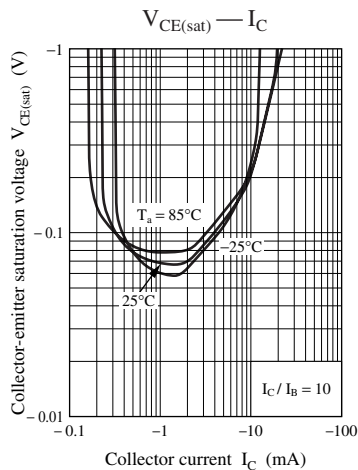
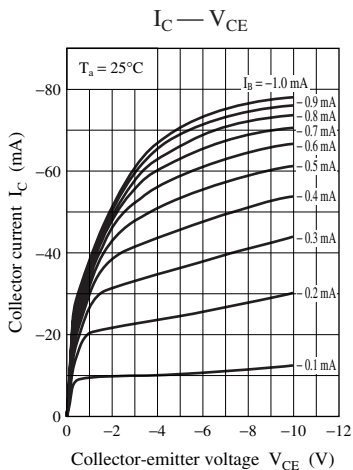
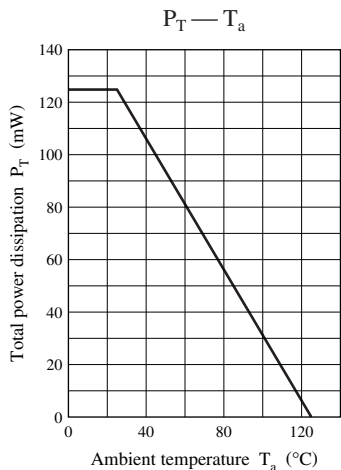
2. \*: Ratio between one and another



Marking Symbol: 1P

Internal Connection





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